

Notice of References Cited	Application/Control No. 10/734,905		Applicant(s)/Patent Under Reexamination HWANG ET AL.	
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	C	US-6,557,144 B1	04-2003	Lu et al.	716/2
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	V	Cong et al., "Structural Gate Decomposition for Depth-Optimal Technology Mapping in LUT-Based FPGA Design", June 1996, IEEE Design Automation Conference Proceedings, pp. 726 - 729.			
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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